



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/164,898	10/01/1998	JAMES AKIYAMA	42390.P3373	7208

7590 09/12/2003

JAMES H SALTER  
BLAKELY SOKOLOFF TAYLOR & ZAFMAN  
12400 WILSHIRE BOULEVARD  
7TH FLOOR  
LOS ANGELES, CA 90025

EXAMINER

VITAL, PIERRE M

ART UNIT

PAPER NUMBER

2188

DATE MAILED: 09/12/2003

30

Please find below and/or attached an Office communication concerning this application or proceeding.

30

**Advisory Action**

Application No.

09/164,898

Applicant(s)

AKIYAMA, JAMES

Examiner

Pierre M. Vital

Art Unit

2188

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 25 August 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

**PERIOD FOR REPLY [check either a) or b)]**

a)  The period for reply expires 3 months from the mailing date of the final rejection.  
b)  The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.  
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1.  A Notice of Appeal was filed on \_\_\_\_\_. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2.  The proposed amendment(s) will not be entered because:
  - (a)  they raise new issues that would require further consideration and/or search (see NOTE below);
  - (b)  they raise the issue of new matter (see Note below);
  - (c)  they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
  - (d)  they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_.

3.  Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.
4.  Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5.  The a) affidavit, b) exhibit, or c) request for reconsideration has been considered but does NOT place the application in condition for allowance because: see attached
6.  The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7.  For purposes of Appeal, the proposed amendment(s) a) will not be entered or b) will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: none.Claim(s) objected to: none.Claim(s) rejected: 19-37.Claim(s) withdrawn from consideration: none.

8.  The proposed drawing correction filed on \_\_\_\_\_ is a) approved or b) disapproved by the Examiner.

9.  Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_.

10.  Other: see attached

*Reginald G. Bragdon*  
REGINALD G. BRAGDON  
PRIMARY EXAMINER

***Response to Arguments***

Applicant's arguments filed August 25, 2003 have been fully considered but they are not persuasive. As to the remarks, Applicant asserted that:

(a) The prior art of record does not teach or suggest an IDE interface coupled to a system bus that receives disk drive requests from BIOS via the system bus.

Examiner respectfully traverses applicant's arguments for the following reasons.

Examiner would like to point out that Cheng discloses a system bus (i.e., *ISA bus 135*) coupled to an IDE interface (i.e., *IDE interface 110*). It should be borne in mind that, in discussions of electrical components, the terms "connected", "operatively connected", "electrically connected", and like terms denote an electrical path between two components. It is understood, however, that such terms do not preclude the existence of additional components interposed between the two original components, even if an additional such component has the capability of interrupting or affecting signal or data transmission between the two original components. Only through the use of the term "directly connected", or like terms, is it intended to denote an electrical connection between two components that precludes any additional components, other than an electrical conductor, interposed between the two original components.

Cheng further discloses an IDE interface that receives disk drive requests from BIOS via the system bus as detailed in column 6, lines 4-35 and Fig. 1. The BIOS 140 is coupled to the ISA bus 135, which is employed as an I/O bus, i.e., system bus (see

*column 6, lines 4-10).* Furthermore, Cheng discloses that read/write request from the BIOS 140 is received from the ISA bus 135 (see *column 6, lines 34-35*).

Thus, it can be clearly seen that Cheng discloses an IDE interface coupled to a system bus (*IDE interface 110 coupled to ISA bus 135*) that receives disk drive requests from a BIOS via the system bus (*BIOS receives read/write requests from ISA bus 135*).

(b) The prior art of record does not teach or suggest a bus interface that communicates directly with BIOS.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a bus interface that communicates directly with BIOS) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The claims as recited do not disclose that a bus interface communicates directly with BIOS. Examiner would like to suggest that applicant amends the independent claims to recite that a bus interface communicates directly with BIOS.